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EXAMINER	
MEONSKE, TONIA L	

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2183	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/871,301	DALLY ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18 and 19* is/are allowed.

6)☒ Claim(s) *1-17,and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed August 13, 2001 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because no publication date has been provided for the Cormen et al. reference. The information in the Cormen et al. reference referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

3. The oath or declaration is defective because:

a. Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-9, 15-17, 22-24, and 26 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Asai et al., US Patent 5,553,309.

7. Referring to claim 1, Asai et al. have taught a method of performing a conditional vector output operation in a processor, the method comprising:

a. receiving electrical signals representative of an input vector (Figure 6, input vector register 1);

b. receiving electrical signals representative of a condition vector (Figure 6, mask register), the number of values in the input vector being equal to the number of values in the condition vector, values in the input vector and in the condition vector being in one-to-one correspondence with one another (Figure 6, The input vector register 1 and the mask register each have ten elements in one-to-one correspondence with one another.), and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input vector (Figure 6, mask register, mask generation 601, column 13, lines 57-67);

c. generating electrical signals representative of an output vector containing values in the input vector for which corresponding values in the condition vector are equal to a predetermined value (Figure 6, output vector register 2), a length of the output vector being equal to a number of values in the condition vector that are equal to the predetermined value (Figure 6, element output vector register 1, Six bits with the value of

one are in the mask register and six values equal to one appear in the output vector register 2.).

8. Referring to claim 2, Asai et al. have taught the method of claim 1, as described above, and wherein the predetermined conditional expression is a Boolean expression (Figure 6, mask register, mask generation 601column 13, lines 57-67).

9. Referring to claim 3, Asai et al have taught the method of claim 1, as described above, and further comprising:

a. generating electrical signals representative of at least one additional output vector containing values in the input vector for which corresponding values in the condition vector are not equal to the predetermined value (Figure 6, output vector register 3), wherein a plurality of output vectors comprise the output vector (Figure 6, element output vector register 2) and the at least one additional output vector (output vector register 3).

10. Referring to claim 4, Asai et al. have taught the method of claim 3, as described above, and wherein each value in the input vector is in one and only one of the plurality of output vectors (Figure 6, each value in input vector register 1 appears only in one of the output vector register 2 or output vector register 3.).

11. Referring to claim 5, Asai et al. have taught the method of claim 3, as described above, and wherein generating the plurality of output vectors includes, for each value in the condition vector, including one of the corresponding values in the input vector in one of the plurality of output vectors (Figure 6, Values from the input vector register 1 are moved to either the output vector register 2 or the output vector register 3.).

12. Referring to claim 6, Asai et al. have taught the method of claim 3, as described above, and further comprising:

a. processing portions of the electrical signals corresponding to each of the plurality of output vectors using the processor, the processing for at least two of the output vectors being different from one another (Figure 6 and Figure 7, Vector registers 2 and 3 are stored at different locations in memory.).

13. Referring to claim 7, Asai et al. have taught a method of performing a conditional vector output operation in a processor, the method comprising:

a. receiving electrical signals representative of an input vector (Figure 6, input vector register 1);

b. receiving electrical signals representative of a condition vector, the number of values in the input vector being equal to the number of values in the condition vector (Figure 6, element mask register), values in the input vector and in the condition vector being in one-to-one correspondence with one another (Figure 6, The input vector register 1 and the mask register each have ten elements in one-to-one correspondence with one another.), and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input vector (Figure 6, mask register, mask generation 601, column 13, lines 57-67);

c. generating electrical signals representative of an output vector containing values in the input vector for which corresponding values in the condition vector are equal to a predetermined value (Figure 6, output vector register 2, Six bits with the value of one are

in the mask register and six values equal to one appear in the output vector register 2.); and

d. storing successive values of the output vector in successive locations in a memory device so that a number of locations in the memory device occupied by stored values of the output vector is equal to a length of the output vector (Figures 6 and 7, Vector register 2 is stored in memory.).

14. Referring to claim 8, Asai et al. have taught a method of performing a conditional vector output operation in a processor, the method comprising:

a. receiving electrical signals representative of an input vector (Figure 6, input vector register 1);

b. receiving electrical signals representative of a condition vector, the number of values in the input vector being equal to the number of values in the condition vector (Figure 6, mask register), values in the input vector and in the condition vector being in one-to-one correspondence with one another (Figure 6, The input vector register 1 and the mask register each have ten elements in one-to-one correspondence with one another.), and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input vector (Figure 6, mask register, mask generation 601, column 13, lines 57-67);

c. generating electrical signals representative of an output vector containing values in the input vector for which corresponding values in the condition vector are equal to a predetermined value (Figure 6, output vector register 2); and

d. storing successive values of the output vector in successive locations in a memory device so that a number of locations in the memory device occupied by stored values of the output vector is equal to the number of values in the input vector for which corresponding values in the condition vector are equal to the predetermined value (Figures 6 and 7, Vector register 2 is stored in memory.).

15. Referring to claim 9, Asai et al. have taught a method of performing a conditional vector output operation in a parallel processor having a plurality of clusters therein, the method comprising:

a. receiving electrical signals representative of an input vector (Figure 6, input vector register 1);

b. receiving electrical signals representative of a condition vector (Figure 6, mask register), the number of values in the input vector being equal to the number of values in the condition vector, values in the input vector and in the condition vector being in one-to-one correspondence with one another (Figure 6, The input vector register 1 and the mask register each have ten elements in one-to-one correspondence with one another.), and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input vector (Figure 6, mask register, mask generation 601, column 13, lines 57-67);

c. using the clusters to generate electrical signals representative of an output vector containing values in the input vector for which corresponding values in the condition vector are equal to a predetermined value (Figure 6, output vector register 2, The input vector register and the mask register are the clusters.); and

d. storing a value of the output vector in a cluster different from a cluster which generated that value (Figure 6, The output vector is stored in the output vector register2 which is a cluster different from a cluster which generated that value.).

16. Referring to claim 15, Asai et al. have taught a method of performing a conditional vector switching operation in a processor, the method comprising:

a. receiving electrical signals representative of an input vector, the input vector having input vector elements (Figure 6, element input vector register 1);

b. receiving electrical signals representative of a condition vector, the condition vector having condition vector elements (Figure 6, mask register), a number of the input vector elements being equal to a number of the condition vector elements, the input vector elements and the condition vector elements being in one-to-one correspondence with one another (Figure 6, There are ten elements in the mask register that are in one-to-one correspondence with the ten elements in the input vector register 1.), and each condition vector element being a result of evaluating a predetermined conditional expression using data corresponding to an input vector element (Figure 6, mask register, mask generation 601, column 13, lines 57-67);

c. generating electrical signals representative of an intermediate vector (Figure 6, input vector register 1), the intermediate vector having intermediate vector elements that contain input vector elements for which corresponding condition vector elements are equal to a predetermined value (Figure 6, The six elements in the output vector register 2 are the input vector register 1 values which correspond to the predetermined value of one in the mask register.), a number of intermediate vector elements being equal to a number

of condition vector elements in the condition vector that are equal to the predetermined value (Figure 6); and

d. generating electrical signals representative of an output vector (Figure 7, Element 604 generates signals to store the output vector in memory.), the output vector having output vector elements in one-to-one correspondence with the intermediate vector elements, each output vector element is a result of a computation performed on each corresponding intermediate vector element (Figure 7, The vector register 2 elements are stored in memory as a result of a vector storing computation.).

17. Referring to claim 16, Asai et al. have taught a method of performing a conditional vector switching operation in a processor, the method comprising:

a. receiving electrical signals representative of an input vector of a first length, the input vector having input vector elements (Figure 6, input vector register 1);

b. receiving electrical signals representative of a condition vector of a second length (Figure 6, element mask register), the first and second lengths being equivalent (Figure 6, The mask register and the input vector register 1 both have equivalent lengths.), the condition vector having condition vector elements in one-to-one correspondence with the input vector elements (Figure 6, mask register, input vector register 1), at least one of the condition vector elements being equal to a value other than a predetermined value (Figure 6, The mask register has four elements equal to zero, which is not the predetermined value.), at least one of the condition vector elements being equal to the predetermined value (Figure 6, The mask register has six elements equal to one, or a predetermined value.);

c. generating electrical signals representative of an intermediate vector of a third length, the third length being less than the first length, the intermediate vector having intermediate vector elements in one-to-one correspondence with any condition vector elements being equivalent to the predetermined value, the intermediate vector elements respectively comprising any input vector elements corresponding to any condition vector elements that are equal to the predetermined value (Figure 6, The output vector register 2 is the intermediate vector.); and

d. performing a computation on each intermediate vector element to generate electrical signals representative of an output vector of a fourth length, the third and fourth lengths being equivalent (Figure 7, A vector storing computation is performed on the vector register 2 values in order to store the values in memory.).

18. Referring to claim 17, Asai et al. have taught a method of performing a conditional vector switching operation in a processor, the method comprising:

a. receiving electrical signals representative of an input vector, the input vector having input vector elements (Figure 6, input vector register 1);

b. receiving electrical signals representative of a condition vector, the condition vector having condition vector elements, a number of the input vector elements being equal to a number of the condition vector elements, the input vector elements and the condition vector elements being in one-to-one correspondence with one another (Figure 6, The mask register is the condition vector.), and each condition vector element being a result of evaluating a predetermined conditional expression using data corresponding to

an input vector element (Figure 6, mask register, mask generation 601, column 13, lines 57-67);

c. generating electrical signals representative of a first intermediate vector, the first intermediate vector having first intermediate vector elements that contain input vector elements for which corresponding condition vector elements are equal to a first predetermined value, a number of first intermediate vector elements being equal to a first number of condition vector elements in the condition vector that are equal to the first predetermined value (Figure 6, output vector register 2); and

d. generating electrical signals representative of a second intermediate vector, the second intermediate vector having second intermediate vector elements that contain input vector elements for which corresponding condition vector elements are equal to a second predetermined value, a number of second intermediate vector elements being equal to a second number of condition vector elements in the condition vector that are equal to the second predetermined value (Figure 6, output vector register 3);

e. generating electrical signals representative of a first output vector, the first output vector having first output vector elements in one-to-one correspondence with the first intermediate vector elements, each first output vector element is a result of a first computation performed on each corresponding first intermediate vector element (Figure 7, Vector register 2 is stored in memory as a first output vector.); and

f. generating electrical signals representative of a second output vector, the second output vector having second output vector elements in one-to-one correspondence with the second intermediate vector elements, each second output vector element is a result of

a second computation performed on each corresponding second intermediate vector element (Figure 7, Vector register 3 is stored in memory as a second output vector.).

19. Referring to claim 22. A processor comprising:

a. a first memory area to store input vector elements (Figure 6, input vector register 1);

b. a second memory area to store condition vector elements, the second memory area having a same length as the first memory area (Figure 6, mask register);

c. a third memory area to store output vector elements, the third memory area having a length equal to a number of condition vector elements that are equal to a predetermined value (Figure 6, output vector register 2); and

d. a logic circuit that transfers input vector elements from the first memory area to the third memory area when corresponding condition vector elements stored in the second memory area are equal to the predetermined value (Figure 6, column 13, line 57-column 14, line 8).

20. Referring to claim 23, Asai et al. have taught a processor comprising:

a. a first memory area to store input vector elements (Figure 6, input vector register 1);

b. a second memory area to store condition vector elements, the second memory area having a same length as the first memory area (Figure 6, mask register);

c. a third memory area to store output vector elements, the third memory area having a length equal to a number of condition vector elements that are equal to a predetermined value (Figure 6, output vector register 2); and

d. a logic circuit that transfers input vector elements from the first memory area to the third memory area when corresponding condition vector elements stored in the second memory area are equal to the predetermined value so that a number of locations in the third memory area occupied by the output vector elements stored in the third memory area is equal to a number of input vector elements for which corresponding condition vector elements are equal to the predetermined value (Figure 6, column 13, line 57-column 14, line 8).

21. Referring to claim 24, Asai et al. have taught a processor comprising:

a. a first memory area to store input vector elements (Figure 6, input vector register 1);

b. a second memory area to store condition vector elements, the second memory area having a same length as the first memory area (Figure 6, mask register);

c. a third memory area to store output vector elements, the third memory area comprising memory locations from plural clusters, the plural clusters generating the output vector elements, the third memory area having a length equal to a number of condition vector elements that are equal to a predetermined value (Figure 6, output vector register 2); and

d. a logic circuit that transfers input vector elements from the first memory area to the third memory area when corresponding condition vector elements stored in the second memory area are equal to the predetermined value to generate the output vector elements in the plural clusters, wherein an output vector element is stored in a memory

location of a different cluster of the plural clusters than that cluster which generated the output vector element (Figure 6, column 13, line 57-column 14, line 8).

22. Referring to claim 26, Asai et al. have taught a processor to perform conditional vector operations, including a conditional vector input operation and a conditional vector output operation, comprising:

a. a first memory area to store an input vector stream, the input vector stream having input vector elements (Figure 1, element 1 which is referred to as element 10 in the text of the patent, main storage);

b. a second memory area to store an output vector stream, the output vector stream having output vector elements (Figure 1, element 1 which is referred to as element 10 in the text of the patent, main storage);

c. a third memory area to store a condition vector stream, the condition vector stream having condition vector elements (Figure 6, mask register);

d. a buffer having a first plurality of entries and a second plurality of entries to store the input vector elements (Figure 1, element 3, Figure 6, input vector register 1) and the output vector elements (Figure 1, element 3, Figure 6, output vector register 2);

e. a plurality of processing elements to process input vector elements into output vector elements (Column 13, line 53-column 14, line 25, Figure 5, elements 506 and 507);

f. a switch configured to transfer the input vector elements from the buffer to the processing elements and to transfer the output vector elements to the buffer (Figure 5, Figure 6, elements 502, 503, 505, 506, and 507, Column 13, line 53-column 14, line 25),

the buffer receiving the input vector elements from the first memory area (Figure 6, input vector register 1), the buffer receiving the output vector elements from the plurality of processing elements via the switch (Figure 6, output vector register 2), the second memory area reading the output vector elements from the buffer (Figure 5, the output vector register are written to memory), and the plurality of processing elements reading the input vector elements from the buffer via the switch in accordance with the condition vector elements (Figure 5, elements 506 and 507, Figure 6, mask register, Column 13, line 53-column 14, line 25); and

g. a controller to direct conditional vector input and output operations by controlling reading the input and the output vector elements from the buffer, by controlling receiving the input and the output vector elements into the buffer (Figure 6, input vector register 1 and output vector register 2); by processing the condition vector elements (Figure 6, compress the vector, element 602), and by configuring the switch so that the switch is capable of transferring the input and output vector elements between any of the first plurality of entries of the buffer, any of the second plurality of entries of the buffer, and any of the plurality of processing elements (Figures 5 and 6, column 13, line 53-column 14, line 25).

23. Claims 10-14, 20, 21, and 25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Inagami et al., US Patent 4,881,168.

24. Referring to claim 10, Inagami et al. have taught a method of performing a distributed conditional vector input operation in a processor, the method comprising:

a. generating a plurality of electrical signals as a condition vector representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data (Figure 4, element 22);

b. distributing a plurality of electrical signals as an input vector having input vector elements to arithmetic clusters in the plurality of arithmetic clusters for which a corresponding portion of the condition vector is equal to a predetermined value (Figure 4, element 21, column 6, line 37-column 7, line 13), a length of the condition vector being greater than a length of the input vector (Figure 4, elements 21 and 22, The condition vector, element 22, has a length of sixteen and the input vector has a length of ten.);

c. using the arithmetic clusters to process the input vector elements distributed thereto (column 6, line 37-column 7, line 13, The sub-pipes are the clusters.); and

d. assembling the processed input vector elements to form an output vector having a length equal to that of the condition vector (Figure 4, element 23).

25. Referring to claim 11, Inagami et al. have taught a method according to claim 10, as described above, and wherein the corresponding portion of the condition vector comprises corresponding condition vector elements (Figure 4, element 22), and wherein a certain plurality of arithmetic clusters receive input vector elements as a result of corresponding condition vector elements for the certain plurality of arithmetic clusters being equal to the predetermined value (column 6, line 37-column 7, line 13, Certain sub-pipes, or clusters, receive input vector elements as a result of the corresponding condition vector elements.).

26. Referring to claim 12, Inagami et al. have taught a method of performing a conditional vector input operation in a processor, the method comprising:

a. generating a plurality of electrical signals as a condition vector representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data (Figure 4, element 22, column 6, line 37-column 7, line 13);

b. providing a plurality of electrical signals as an input vector having input vector elements (Figure 4, element 21) to arithmetic clusters in the plurality of arithmetic clusters for which corresponding condition vector elements of the condition vector are equal to a predetermined value (column 6, line 37-column 7, line 13), the number of clusters being greater than the number of input vector elements (Figure 4, column 6, line 37-column 7, line 13, There are ten input vector elements and sixteen clusters, or sub-pipes.), the input vector elements being in one-to-one correspondence with corresponding condition vector elements of the condition vector that are equal to the predetermined value (Figure 4, column 6, line 37-column 7, line 13, Values in element 21 are in one-to-one correspondence with the values of one on the mask vector 22.);

c. using the arithmetic clusters to process the input vector elements provided thereto (column 6, line 37-column 7, line 13, The sub-pipes process the input vector elements); and

d. assembling the processed input vector elements to form an output vector (Figure 4, element 23).

27. Referring to claim 13, Inagami et al. have taught a method of performing a conditional vector input operation in a processor, the method comprising:

a. generating a plurality of electrical signals as a condition vector representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data (Figure 4, element 22, column 6, line 37-column 7, line 13);

b. providing a plurality of electrical signals as an input vector having input vector elements to arithmetic clusters in the plurality of arithmetic clusters for which corresponding condition vector elements of the condition vector are equal to a predetermined value (Figure 4, column 6, line 37-column 7, line 13), the number of clusters being greater than the number of input vector elements (Figure 4, column 6, line 37-column 7, line 13, There are ten input vector elements and sixteen clusters, or sub-pipes.), the input vector having only input vector elements corresponding to condition vector elements of the condition vector that are equal to the predetermined value (Figure 4, column 6, line 37-column 7, line 13, Values in element 21 are in one-to-one correspondence with the values of one on the mask vector 22.);

c. using the arithmetic clusters to process the input vector elements provided thereto (column 6, line 37-column 7, line 13, sub-pipes); and

d. assembling the processed input vector elements to form an output vector (Figure 4, element 23).

28. Referring to claim 14, Inagami et al. have taught a method of performing a distributed conditional vector input operation in a processor, the method comprising:

a. generating a plurality of electrical signals as a condition vector representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data (Figure 4, element 22, column 6, line 37-column 7, line 13);

b. distributing a plurality of electrical signals from a storage area in at least one cluster as an input vector (Figure 4, element 21) to arithmetic clusters in the plurality of arithmetic clusters for which a corresponding portion of the condition vector is equal to a predetermined value (column 6, line 37-column 7, line 13, Vectors are distributed to the sub-pipes based on equality of the mask vector.), a length of the condition vector being greater than a length of the input vector (Figure 4, Elements 22 and 21, The mask vector has 16 elements and the input vector has 10 elements.);

c. using the arithmetic clusters to process input vector elements of the input vector distributed thereto (column 6, line 37-column 7, line 13, sub-pipes);

d. assembling the processed input vector elements to form an output vector having a length equal to that of the condition vector (Figure 4, element 23); and

e. storing an output vector element of the output vector in a storage area of a cluster different from a cluster from which an input vector element was distributed (Figure 4, The output vector is stored in a vector register and the input vector is stored in the main storage.).

29. Referring to claim 20 Inagami et al. have taught a method of performing a distributed conditional vector load balancing operation in a processor, the method comprising:

a. distributing a plurality of electrical signals as an input vector (Figure 4, element 21), the input vector having input vector elements (Figure 4, $a_0 - a_9$), to successive arithmetic clusters in a plurality of arithmetic clusters (column 6, line 37-column 7, line 12, sup-pipes);

b. using the arithmetic clusters to process the input vector elements distributed thereto, each arithmetic cluster completing processing of one input vector element before another input vector element is distributed to the arithmetic cluster (column 6, line 37-column 7, line 12, sup-pipes), the processing time of any input vector element being dependent on a value of the input vector element (Figure 4, The processing time of the vector elements depends on the value of the input vector element's mask vector.); and

c. assembling the processed input vector elements to form output vector elements of an output vector (Figure 4, element 23), each processed input vector element forming at least one output vector element (Figure 4, element 23, column 6, line 37-column 7, line 12).

30. Referring to claim 21, Inagami et al. have taught a method of performing a distributed conditional vector load balancing operation in a processor, the method comprising:

a. distributing a plurality of electrical signals as an input vector, the input vector having input vector elements, to successive processing elements in a plurality of processing elements (Figure 4, element 21); and

b. generating a plurality of electrical signals representative of an output vector, the output vector having output vector elements (Figure 4, element 23); and

c. for any input vector element,

i. requesting the input vector element from the input vector (column 6, lines 37-53, The mask vector requests a_0 from the input vector.);

ii. reading the input vector element into one processing element of the plurality of processing elements (column 6, lines 37-53, a_0 is read into sub-pipe 2-0.);

iii. processing the input vector element for at least one iteration (column 6, lines 37-53);

iv. generating at least one output vector element from the processed input vector element (Figure 4, element 23);

v. reading an immediately succeeding input vector element, if available, of the input vector elements into any successive processing element of the plurality of processing elements that has completed processing any input vector element (column 6, lines 53-63, a_4 is read into sub-pipe 2-0);

vi. requesting a successive input vector element, if available, of the input vector elements (column 6, lines 53-63, The mask vector requests a_4 from the input vector.); and

vii. reading the successive input vector element into the one processing element when the input vector element has been processed (column 6, line 48-column 7, line 13).

31. Referring to claim 25, Inagami et al. have taught a processor comprising:

a. a first memory area to store input vector elements (Figure 4, element 21)

b. a second memory area to store condition vector elements, the first memory area having a length equal to a number of condition vector elements that are equal to a predetermined value (Figure 4, element 22); and

c. a third memory area to store output vector elements, the third memory area having a same length as the second memory area (Figure 4, element 23); and

d. a logic circuit that transfers input vector elements from the first memory area to the third memory area when corresponding condition vector elements stored in the second memory area are equal to the predetermined value (Figure 4, column 6, line 32-column 7, line 13).

Allowable Subject Matter

32. Claims 18 and 19 are allowed.

Conclusion

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tlm

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